IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: BEAUJOIN ET AL.	)	
Serial No. 10/075,113	)	Examiner: J. TABONE, JR
Confirmation No: 6957	)	Art Unit: 2133
Filing Date: FEBRUARY 13, 2002	)	
For: METHOD OF TESTING A SEQUENTIAL ACCESS MEMORY PLANE AND A CORRESPONDING SEQUENTIAL ACCESS MEMORY SEMICONDUCTOR DEVICE	)	

APPELLANTS' REPLY BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Herewith is Appellants' Reply Brief that is submitted in reply to the Examiner's Answer to Appellants' Appeal Brief. If any additional extensions and/or fees are required, authorization is given to charge Deposit Account No. 01-0484.

A. Status of the Claims

Claims 9-31 are pending in the application. Claims 1-8 were canceled. Claims 10, 13, 18, 19, 24, 25, 30 and 31 are objected to, and Claims 9, 11, 12, 14-17, 20-23 and 26-29 are rejected. In the Office Action mailed March 7, 2006, and in response to the arguments set forth in Appellants' original brief, filed December 21, 2005, the Examiner withdrew the previous rejection of Claims 10, 13, 18, 19, 24, 25, 30 and 31. The

rejection of Claims 9, 11, 12, 14-17, 20-23 and 26-29 is being appealed herein.

B. Grounds of Rejection to be Reviewed On Appeal

Claims 9, 11, 14-17, 20-23 and 26-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Kim et al. (U.S. Patent No. 6,108,802) in view of Martens (U.S. Patent No. 5,751,727); Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Kim et al. in view of Martens and further in view of Zorian et al. (U.S. 6,330,696). Claims 9, 11, 12, 14-17, 20-23 and 26-29 stand together as a group.

C. Arguments

The claimed invention is directed to the testing of a sequential access memory array with a particularly simple implementation leading to a small overall size of the test logic.

Appellants emphasize that the independent claims include testing a sequential access memory plane by writing test words each made up of test bits in the memory array, and then sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word. It is this combination of features which is not fairly taught or suggested in the cited references and which patentably defines over the cited references.

As pointed out in the Appeal Brief, the method/device of Kim et al. includes the use of an output data evaluator (ODE) that receives the data output on the data output (DO) line. However, contrary to the Examiner's assertion in the Examiner's Answer, there is no teaching of extracting the test words and comparing corresponding test bits with expected data bits.

Kim et al. specifically teaches that the output data compacted by the ODE 120 during test intervals takes the form of responses generated by the RAM 102 to the test patterns. Not only does the Kim et al. reference fail to teach sequentially extracting test words from the memory plane and sequentially comparing the test bits with the expected binary data bits, as claimed; but, the reference also fails to teach the features specifically relied upon by the Examiner.

Additionally, although the Examiner goes to great lengths to explain his understanding of the terms "scan", "serial" and "sequential", there is no clear teaching of the presently claimed features in the cited references as relied upon by the Examiner in the rejection. Martens teaches that the array has the capability of reading data out serially in certain testing conditions (e.g. column 5). As such the memory elements are connected in series. However, nothing in Martens discloses testing a sequential access memory plane by sequentially extracting test words from the memory plane to sequentially compare test bits with expected binary data bits, as claimed.

It can be clearly seen in FIG. 4 of Martens that the output of the last memory element 108 is sent to a test circuit.

However, nothing in any of the disclosure of Martens teaches sequentially extracting test words from the memory plane and sequentially comparing the test bits with expected binary data bits, as claimed. There is no teaching that the output of the last memory element 108 includes sequentially extracted test words or that the test circuit (not shown in FIG. 4 of Martens) sequentially compares test bits with respective expected data bits.

Accordingly, as pointed out in the Appeal Brief, the Examiner's hypothetical combination of Kim et al. and Martens, even if obvious, cannot meet the features of the claimed invention. Such a combination of teachings could at most result in the testing method and device of Kim et al. including the scannable latch circuit array of Martens. As set forth in detail above, this is not enough to meet the claimed features of the invention which requires sequentially extracting the test words from the memory array and, for each extracted test word, sequentially comparing the corresponding test bits with expected data bits, before extracting the next test word.

Accordingly, for at least the reasons given above, Appellants maintain that the cited references do not disclose or fairly suggest the invention as set forth in independent Claims 9, 11, 14, 20 and 26. Thus, the rejections under 35 U.S.C. §103(a) should be reversed. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above.

D. Conclusion

In view of Appellants' reply to the Examiner's arguments, it is respectfully submitted that all of the claims are patentable over the prior art. Appellants, therefore, respectfully request that the Board of Patent Appeals and Interferences reverse the earlier unfavorable decision of the Examiner.

Respectfully submitted,

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